1. A method for maintaining the stoichiometry of a high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a high dielectric constant thin film material on said substrate; and

doping said high dielectric thin film material with a dopant by ion implantation, wherein said high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

2. The method according to claim 1, wherein said high dielectric thin film material is doped by varying the implant angle of the dopant.

3. The method according to claim 2, wherein said high dielectric constant thin film material is selected from the group consisting of BST, SBT, $SrTiO_3$ and PZT.

4. The method according to claim 3, wherein said high dielectric constant thin film material is BST.

5. The method according to claim 4, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

6. The method according to claim 2, wherein said high dielectric constant thin film material is a pervoskite of the formula ABO_3 where A represents metals selected from Ba, Bi, Sr, Pb, Ca, and La, and B represents metals selected from Ti, Zr, Ta, Mo, W, and Nb.

7. The method according to claim 6, wherein said doping step includes doping the A-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ba, Bi, Sr, Pb, Ca, and La.

8. The method according to claim 6, wherein said doping step includes doping the B-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb.

9. The method according to claim 6, wherein said pervoskite is barium strontium titanite and said doping step includes doping the A-site with a dopant selected from the group consisting of Ba, and Sr.

10. The method according to claim 6, wherein said pervoskite is barium strontium titanite and said doping step includes doping the B-site with Ti.

11. The method according to claim 10, wherein said barium strontium titanite is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% in said barium strontium titanite film.

12. The method according to claim 11, wherein the ratio of Ba to Sr is about 70:30.

13. A method for maintaining the stoichiometry of a high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a high dielectric constant thin film material on said substrate;

forming a capping layer over said first level and said second level of said substrate; and

doping said high dielectric thin film material formed on said sidewalls with a dopant by ion implantation, wherein said high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

14. The method according to claim 13, wherein said high dielectric thin film material is doped by varying the implant angle of the dopant.

15. The method according to claim 14, wherein said high dielectric constant thin film material is selected from the group consisting of BST, SBT, $SrTiO_3$ and PZT.

16. The method according to claim 15, wherein said high dielectric constant thin film material is BST.

17. The method according to claim 16, wherein said dopants are selected from the group consisting of barium, strontium and titanium..

18. The method according to claim 14, wherein said high dielectric constant thin film material is a pervoskite of the formula ABO_3 where A represents metals selected from Ba, Bi, Sr, Pb, Ca, and La, and B represents metals selected from Ti, Zr, Ta, Mo, W, and Nb.

19. The method according to claim 18, wherein said doping step includes doping the A-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ba, Bi, Sr, Pb, Ca, and La.

20. The method according to claim 18, wherein said doping step includes doping the B-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb.

21. The method according to claim 18, wherein said pervoskite is barium strontium titanite and said doping step includes doping the A-site with a dopant selected from the group consisting of Ba and Sr.

22. The method according to claim 18, wherein said pervoskite is barium strontium titanite and said doping step includes doping the B-site with Ti.

23. The method according to claim 22, wherein said barium strontium titanite is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% in said barium strontium titanite film.

24. The method according to claim 23, wherein the ratio of Ba to Sr is about 70:30.

25. A method for maintaining the stoichiometry of a BST high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate; and

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material.

26. The method according to claim 25, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

27. The method according to claim 26, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

28. The method according to claim 27, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

29. The method according to claim 27, wherein said BST high dielectric thin film material is doped with Ti.

30. The method according to claim 29, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

31. The method according to claim 30, wherein the ratio of Ba to Sr is about 70:30.

32. A method for maintaining the stoichiometry of a BST high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate;

forming a capping layer over said first and second levels of said substrate; and

doping said BST high dielectric thin film material formed on said sidewalls of said substrate with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

33. The method according to claim 32, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

34. The method according to claim 33, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

35. The method according to claim 34, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

36. The method according to claim 34, wherein said BST high dielectric thin film material is doped with Ti.

37. The method according to claim 36, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

38. The method according to claim 37, wherein the ratio of Ba to Sr is about 70:30.

39. A BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of:

providing a substrate having at least one horizontal component and at least one vertical component;

forming a BST high dielectric constant thin film material on said substrate; and

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material.

40. The BST high dielectric constant thin film material according to claim 39, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

41. The BST high dielectric constant thin film material according to claim 40, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

42. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

43. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is doped with Ti.

44. The BST high dielectric constant thin film material according to claim 43, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. The BST high dielectric constant thin film material according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is included in a DRAM cell.

47. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is formed in a capacitor.

48. A BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate;

forming a capping layer over said first and second levels of said substrate; and

doping said BST high dielectric thin film material formed on said sidewalls of said substrate with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

49. The BST high dielectric constant thin film material according to claim 48, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

50. The BST high dielectric constant thin film material according to claim 49, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

51. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

52. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is doped with Ti.

53. The BST high dielectric constant thin film material according to claim 52, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

54. The BST high dielectric constant thin film material according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

55. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is included in a DRAM cell.

56. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is formed in a capacitor.

57. A method for fabricating a high capacitance thin film integrated circuit capacitor device, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a first electrode on said substrate;

forming a BST high dielectric constant thin film material on said first electrode;

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material; and

forming a second electrode on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

58. The method according to claim 57, wherein said B BST high dielectric thin film material is doped by varying the implant angle of the dopant.

59. The method according to claim 58, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

60. The method according to claim 59, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

61. The method according to claim 59, wherein said BST high dielectric thin film material is doped with Ti.

62. The method according to claim 61, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

63. The method according to claim 62, wherein the ratio of Ba to Sr is about 70:30.

64. The method according to claim 58, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

65. The method according to claim 58, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

66. A method for fabricating a high capacitance thin film integrated circuit capacitor device, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a first electrode on said substrate;

forming a BST high dielectric constant thin film material on said first electrode;

forming a capping layer over said first and second levels of said BST high dielectric constant thin film material;

doping said BST high dielectric thin film material formed on said sidewalls with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped by varying the ion implantation implant angle to maintain the stoichiometry of said BST high dielectric thin film material; and

removing said capping layer and forming a second electrode on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

67. The method according to claim 66, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

68. The method according to claim 67, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

69. The method according to claim 67, wherein said BST high dielectric thin film material is doped with Ti.

70. The method according to claim 69, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

71. The method according to claim 70, wherein the ratio of Ba to Sr is about 70:30.

72. The method according to claim 66, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

73. The method according to claim 66, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

74. An integrated circuit capacitor device comprising:

a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided on said substrate;

a doped BST high dielectric constant thin film material provided on said first electrode, said doped BST high dielectric thin film material being doped to maintain the stoichiometry of said BST high dielectric thin film material; and

a second electrode provided on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

75. The integrated circuit capacitor device according to claim 74, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

76. The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

77. The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with Ti.

78. The integrated circuit capacitor device according to claim 76, wherein said doped BST high dielectric thin film material is doped with Ti to

maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

79. The integrated circuit capacitor device according to claim 78, wherein the ratio of Ba to Sr is about 70:30

80. The integrated circuit capacitor device according to claim 74, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

81. The integrated circuit capacitor device according to claim 74, wherein said integrated circuit capacitor is a container capacitor.

82. The integrated circuit capacitor according to claim 74, wherein said integrated circuit capacitor is formed over a stud.

83. The integrated circuit capacitor according to claim 74, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

84. An integrated circuit comprising:

a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided on said substrate;

a doped BST high dielectric constant thin film material provided on said first electrode, said doped BST high dielectric thin film material being doped by angled ion implantation; and

a second electrode provided on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

85. The integrated circuit capacitor device according to claim 84, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

86. The integrated circuit capacitor device according to claim 85, wherein said doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

87. The integrated circuit capacitor device according to claim 85, wherein said doped BST high dielectric thin film material is doped with Ti.

88. The integrated circuit capacitor device according to claim 86, wherein said doped BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

89. The integrated circuit capacitor device according to claim 88, wherein the ratio of Ba to Sr is about 70:30

90. The integrated circuit capacitor device according to claim 84, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

91. The integrated circuit capacitor device according to claim 84, wherein said integrated circuit capacitor is a container capacitor.

92. The integrated circuit capacitor according to claim 84, wherein said integrated circuit capacitor is formed over a stud.

93. The integrated circuit capacitor according to claim 84, wherein said integrated circuit capacitor is fabricated in a DRAM cell.